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KS82C670/671

Video Clock Generator

Preliminary

FEATURES

- Single/Dual Clock output versions
- Custom (ROM) programmed frequencies up to 100 MHz
- "On-the-fly" frequency selection
- Separate on-chip Phase Locked Loops
- PLL oscillator input from System Bus or 14.31818 MHz Crystal
- External Frequency input operation up to 140MHz
- Low power 1μ CMOS technology

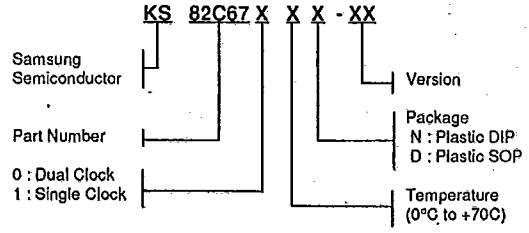
KS82C670

- Two independent clock outputs (Pixel and Memory)
- 32 custom Pixel Clock frequencies (up to 100 MHz)
- 4 custom Memory Clock frequencies (up to 80 MHz)

KS82C671

- Single Pixel Clock output
- 32 custom Pixel Clock frequencies (up to 100 MHz)
- SLEEP input for power down mode
- Latched frequency select inputs

ORDERING INFORMATION



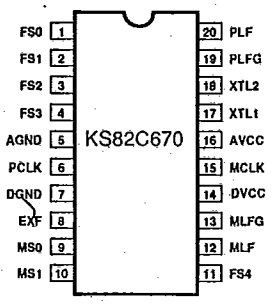
DESCRIPTION

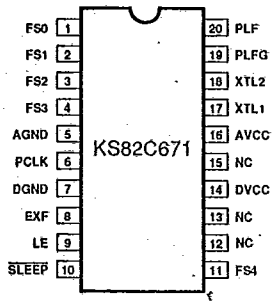
The KS82C670/671 are integrated graphics clock generators which can replace several oscillators and crystals in any application that requires dynamic frequency switching. In a graphics system, one of these devices can be used to generate frequencies for several resolutions. In P.C. VGA systems, all frequencies for previous generation modes, like EGA, CGA and MDA, can be provided in a single device. Up to 32 frequencies for the Pixel Clock, and up to 4 frequencies for the Memory Clock can be specified via factory programmed ROM mask. Each of these frequencies can be accessed on-the-fly by supplying an input address to the device.

An external clock reference must be supplied from a crystal connected to the internal oscillator, or from the 14.31818 MHz bus clock. These devices allow an additional external clock input to be multiplexed with internally generated frequencies to the output. The maximum external clock frequency is 140 MHz.

If required by the application, power down modes and input latching functions are also available by choosing the appropriate pin configuration.

PIN CONFIGURATIONS





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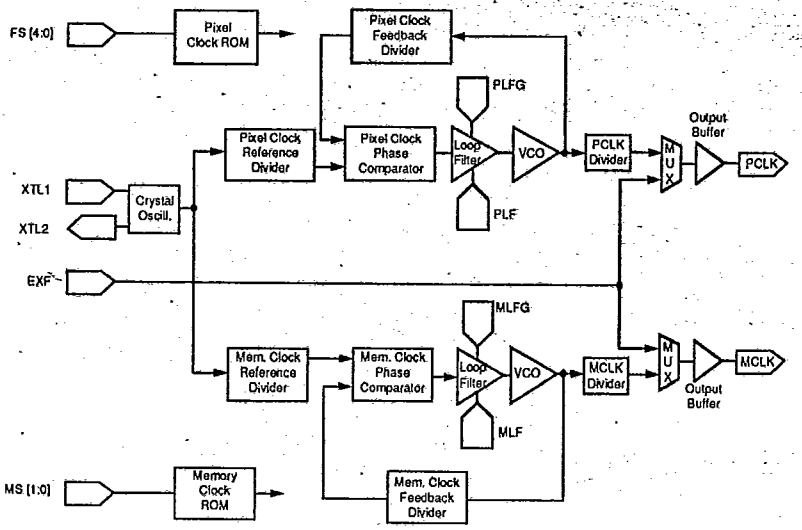
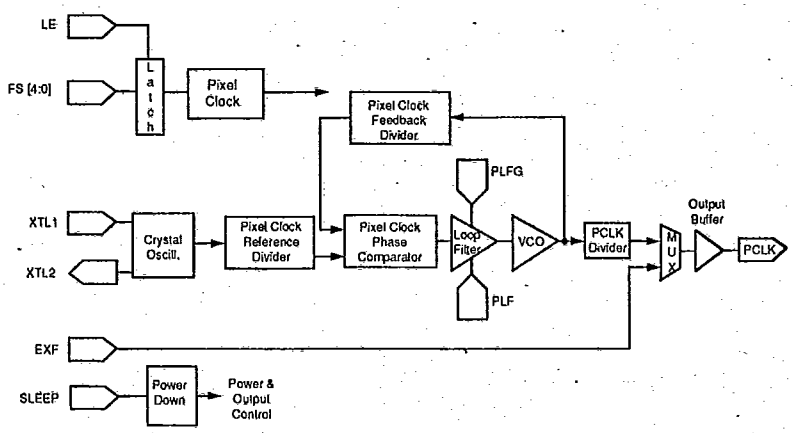
BLOCK DIAGRAMS



KS82C670 Functional Block Diagram



KS82C671 Functional Block Diagram

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INTRODUCTION

The KS82C670/671supports all the frequencies required for low to very high resolution graphics systems:

VGA	14.31818	to	65 MHz
8514/A	25.28	to	44.9 MHz
Higher resolutions	74.16	to	100 MHz

For VGA, this frequency range allows a user to display up to 1024 x 768 pixel resolution. A frequency of 95MHz allows a 1024 x 1024, 71 Hz non-interlaced display to be driven, thus covering the European standard refresh rate.

Typically, the number of frequencies in a given graphics design is usually less than 8. However, since up to 32 frequencies can be specified in a single device, they can be split into 4 sets of 8, enabling the user to use the same device for up to 4 different board designs. This provides inventory efficiency and flexibility for the board manufacturer.

OPERATION

Each of the customer specific frequencies in the Pixel Clock ROM and Memory Clock ROM are selected by the FS0-FS4 and MS0-MS1 input pins respectively. These inputs do not require latching by any external signal, i.e. they operate in a "flow-through mode". However, for systems that require latched inputs, the KS82C671 provides the LE pin. A HIGH on the LE pin latches the FS0-FS4 signals.

The frequency select pins select a new location of the particular ROM. After a propagation delay through the ROM, the new divisor values are held at the pre-load inputs of each of the pertinent divider counters until the previous count decrements to zero.

The divider outputs from the input and feedback paths drive the phase comparator. The phase comparator drives the VCO with a voltage dependent upon the phase difference between the feedback and reference divider outputs. This voltage performs a correction on the VCO frequency, to bring it closer to the target frequency. This corrected frequency clocks the feedback divider, reducing its phase difference from the reference divider output. After several iterations, the phase locked loop locks on to the desired frequency.

CUSTOMIZED FREQUENCIES

In order to facilitate the design of high performance graphics subsystems, the KS82C670/671 can be customized to provide user-specified frequencies. This can be done via mask programming at the factory by Samsung. Up to 32 output frequencies can be specified for PCLK (KS82C670/671) and up to 4 output frequencies for MCLK (KS82C670 only).

SLEEP MODE

In applications where power consumption is important, e.g., laptops, the KS82C671 provides a significant improvement in power management of the system. The KS82C671 can be put in a low power consumption mode by using the SLEEP pin. A low on this pin disables the internal circuitry and forces the Pixel Clock (PCLK) output to a low. As a result, the supply current is reduced to under 1mA. A high on the SLEEP pin brings the part back into normal operation.

APPLICATION

The KS82C670 features two phase locked loops running off the same reference frequency. One generates the desired Pixel clock and the other generates Memory Clock. The Memory Clock can be used to drive the memory interface of a VGA controller or a Graphics processor, e.g. the 8514/A and TI 34010/20. This clock is independent of the Pixel clock, or the display resolution. This unique feature allows a graphics controller or drawing processor to draw at a high rate while displaying low resolutions that require a slow Pixel clock. Conversely, changing to higher resolutions can be accomplished without changing the clock rate of the drawing facilities. The Memory Clock frequency is based upon the maximum clock rate that the graphics controller or processor can run at, and the speed grade of the frame buffer memory ICs being used.

Both devices have the ability of receiving an external clock which is multiplexed with the internally generated frequency. This external frequency can be used for synchronizing the graphics system to an external source like a frame grabber or VCR to superimpose real time video with graphics or text. In the case of the KS82C670, the external clock signal may be routed to the pixel and/or memory clock outputs as a mask option. If this mask option is chosen, the external clock is selected by a specific address on FS0-FS4 and/or MS0-MS1.

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DESIGN CONSIDERATIONS

To meet the challenge of designing a high speed graphics subsystem, the following design criteria must be considered:

1. *Components*
2. *Power Supply Decoupling*
3. *PCB Layout*

1. *Components*
Leaky capacitors should be avoided as they may cause increased noise over changing conditions of temperature and power supply. Monolithic ceramic capacitors are recommended over standard ceramic types.

2. *Power Supply Decoupling*
Normally, logic gates with fast transition times, switching power supplies, and high power analog circuits generate noise in the graphics system. This noise could get coupled on to the power pins of the KS82C670/671 and become a source of jitter on the outputs. To reduce this noise, both the Digital and Analog power pins must have good decoupling.

A. Specifically, there are two ways of connecting the Analog Power and Ground (AVCC and AGND):

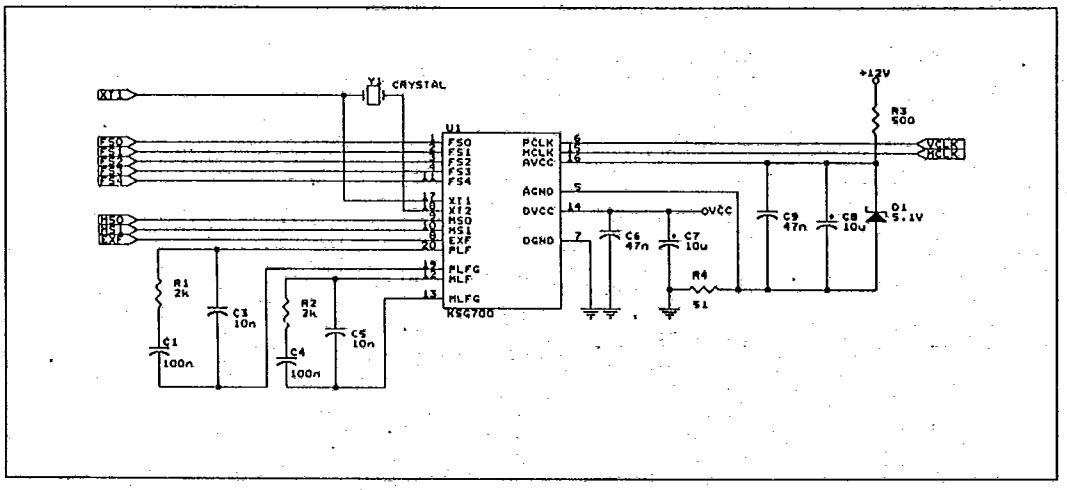
   1. While this configuration is not an absolute requirement, depending upon the particular graphics board, lower noise coupling can be achieved by using a 5.1V zener diode biased through a resistor to the 12V supply. This supply is readily available in the system. See illustration below.

   2. System Ground should be connected to DGND. A 51Ω resistor can be inserted between DGND and AGND to significantly filter noise in the analog power supply to the part. See illustration below.

B. The high frequency supply current to the outputs must be available from the capacitor with the least amount of inductance. For this reason, decoupling capacitors, especially the 47 nF capacitor, should be placed as close as possible to the KS82C670/671.

3. *PCB Layout*
Since both MCLK and PCLK are high frequency signals, they should be separated as much as possible on the PCB board. A good design practice is to place a ground line in between these two signals to reduce the cross talk between them.

Even though careful design techniques have been used to avoid noise coupling into the loop filters, these pins (PLF, MLF) are sensitive to noise in some cases. Care should be taken to avoid digital lines running close to the Loop filter pins (PLF, MLF) and to keep filter components as close to the pins as possible.



Typical Application

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PIN PRESCRIPTION

Pin Number	Name	Type	Description
1, 2, 3, 4, 11	FS [4:0]	I	TTL compatible, Frequency Select inputs (FS0 is the LSB). Used to select 1 out of 32 possible Pixel Clock frequencies.
14	DVCC	P	Digital V_{cc}.
17	XTL1	I	Crystal Input. Alternately, a reference frequency such as the 14.31818 MHz System Bus clock should be connected to this input.
18	XTL2	O	Crystal Output. If an external clock source is connected to XTL1, the XTL2 output should be left unconnected.
8	EXF	I	TTL compatible, External Frequency Input. This frequency can be multiplexed with the internal PLL to the pixel or memory outputs by selecting the proper address.
9, 10 Note 1	MS[1:0]	I	TTL compatible, Memory Clock Select Inputs (MS0 is the LSB). Used to select 1 out of 4 possible Memory Clock frequencies.
15	MCLK	O	TTL compatible, Memory Clock output. This output typically drives a VGA controller memory interface.
12, 13 Note 1	MLF, MLFG	I/O	Memory Clock Loop Filter components connect to these pins.
7	DGND	G	Digital Ground.
6	PCLK	O	TTL compatible, Pixel Dot clock output. This output typically drives the graphics controller.
20, 19	PLF, PLFG	I/O	Pixel Clock Loop Filter components connect to these pins.
5	AGND	G	Analog Ground.
16	AVCC	P	Analog V_{cc}. Generated using 5.1V zener reference or tied directly to DVCC. See application note for details.
9 Note 2	LE	I	TTL compatible, Latch Enable Input. A "HIGH" on this input will latch previously valid data on FS[4:0] frequency select inputs. When LE = "LOW" the latch is transparent.
10 Note 2	$\overline{\text{SLEEP}}$	I	TTL compatible, $\overline{\text{SLEEP}}$ control. A "LOW" on this input forces Pixel Clock and Memory Clock to "LOW". Supply current is reduced to under 1mA.

NOTES:
1. Pin function related to KS82C670 only.
2. Pin function related to KS82C671 only.

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ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to Vss	Vin, Vout	-1 to + 7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-1 to + 7.0	V
Storage Temperature	Tstg	-55 to + 150	°C
Power Dissipation	P_D	0.6	W
Short Circuit Output Current	Ios	50	mA

NOTE:
1. Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0		V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0		0.8	V
Operating Free Air Temperature	T_A	0		70	°C

DC CHARACTERISTICS [0 °C ≤ T_A ≤ 70°C, V_{CC} = 5V ± 10%] (see note)

Parameter	Symbol	Test Conditions	Device	Min	Typ	Max	Unit
Digital Current (Active)	$ICCD_A$	No Output Load	'670			40	mA
			'671			30	
Analog Current (Active)	$ICCA_A$	No Output Load	'670			9	mA
			'671			4.5	
Digital Standby Current	$ICCD_S$	$\overline{SLEEP}$=V_{IL}	'671			1	mA
Analog Standby Current	$ICCA_S$	FS[4:0]=LE=V_{IH}	'671			1	mA
Input Leakage Current	I_{IH}	V_{IN}=5.5V				1	µA
	I_{IL}	V_{IN}=0V		-1			
Input Leakage Current (Pin 9)	I_{IH}	V_{IN}=5.5V	'671			50	µA
	I_{IL}	V_{IN}=0V	'671	-1			
Input Leakage Current (Pin 10)	I_{IH}	V_{IN}=5.5V	'671			1	µA
	I_{IL}	V_{IN}=0V	'671	-50			
Output High Voltage Level	V_{OH}	PCLK ≤ 100MHz; MCLK ≤ 80MHz C_L=30pF (Simulates I_{OH} = -1mA)		2.4			V
Output Low Voltage Level	V_{OL}	PCLK ≤ 100MHz; MCLK ≤ 80MHz C_L= 30pF (Simulates I_{OL} = 1.6mA)				0.4	V

NOTE:
1. Both devices, unless otherwise indicated.

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CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (1, 2, 3, 4, 8, 9, 10, 11)	C_{IN1}			7	pF
Input Capacitance (17)	C_{IN2}			12	pF

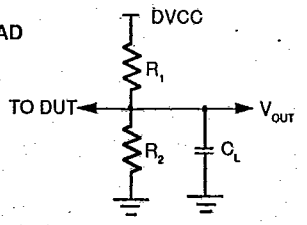
AC CHARACTERISTICS [0 °C ≤ T_A ≤ 70°C, V_{CC} = 5V ± 10%] (see notes)

Parameter	Symbol	Conditions	Device	Min	Typ	Max	Unit
Programmable Frequency Range	F_{PRO}			12.5		100	MHz
Reference Oscillator Frequency	F_{REF}				14.31818		MHz
Output Duty Cycle (T_{ON}/T_{CYC})	DC	R_1 = 1.2 KΩ; R_2 = 2 KΩ, C_L = 30pF		42.5		57.5	%
Nominal Pixel Output Frequency Error	F_{PA}	R_1 = 1.2 KΩ; R_2 = 2 KΩ, C_L = 30pF				0.2	%
Nominal Memory Output Frequency Error	F_{MA}	R_1 = 1.2 KΩ; R_2 = 2 KΩ, C_L = 30pF				TBD	%
Output Frequency Deviation from Nominal over operating range	F_{DEV}	R_1 = 1.2 KΩ; R_2 = 2 KΩ, C_L = 30pF				0.05	%
Output Rise Time	T_R	R_1 = 1.2 KΩ; R_2 = 2 KΩ, C_L = 30pF				4	ns
Output Fall Time	T_F	R_1 = 1.2 KΩ; R_2 = 2 KΩ, C_L = 30pF				4	ns
Latch Enable Set Up Time	T_S		'671	10			ns
Latch Enable Hold Time	T_H		'671	10			ns
Latch Enable Pulse Width	T_{PW}		'671	10			ns
Previous Frequency Valid Time	T_{VPF}			0			ns
New Frequency Settling Time	T_{SNF}					TBD	ns
$\overline{SLEEP}$ ↓ Frequency Disable Time	T_{DIS}		'671	0			ns
$\overline{SLEEP}$ ↑ Frequency Valid Time	T_{VAL}		'671			TBD	%

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	2 to 5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

TEST LOAD



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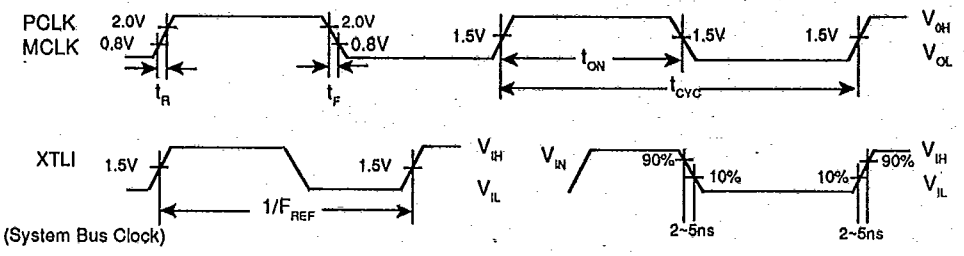
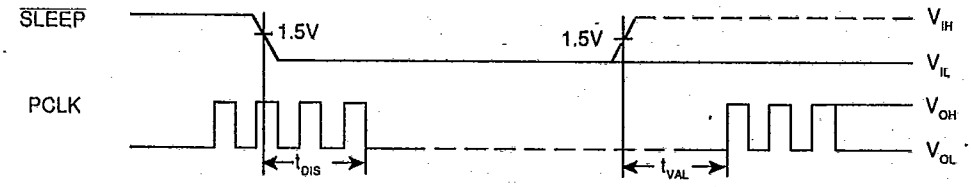
SWITCHING WAVEFORMS

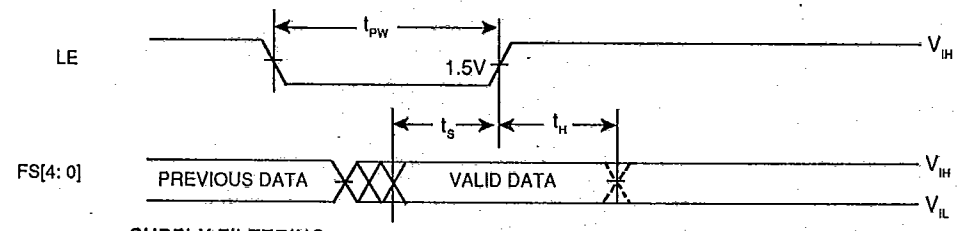
I/O Clocks



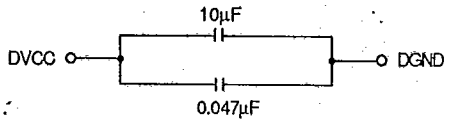
Frequency Disable (KS82C671)

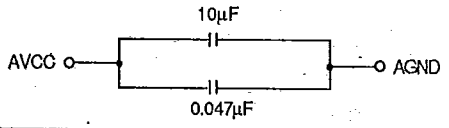


Frequency Select (KS82C671)

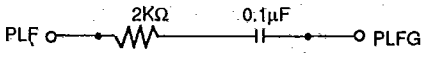


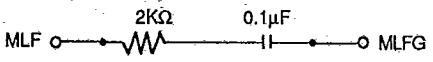
SUPPLY FILTERING





CLOCK FILTERING





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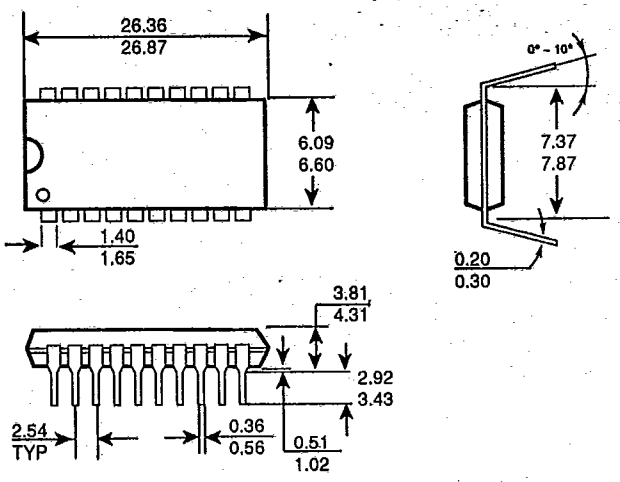
PACKAGE DIMENSIONS

20-Pin DIP

Unit: mm



20-Pin SOP